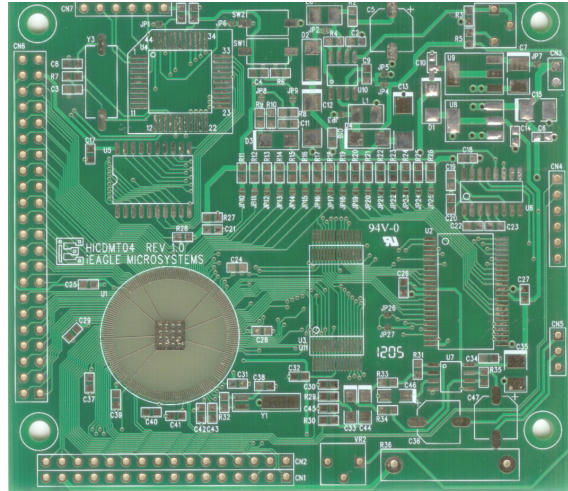
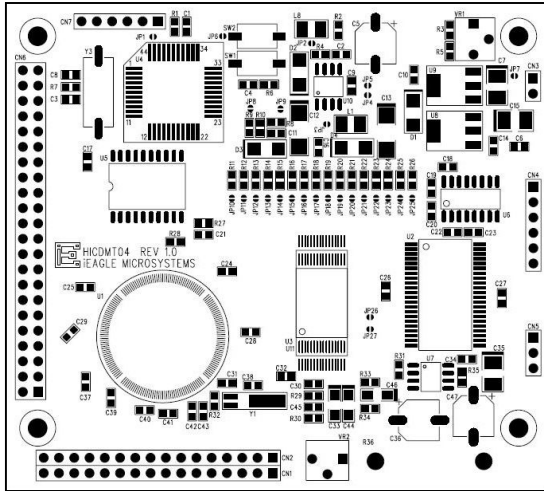




## Graphics Development Board HICDMT04 Layout



### Support for the 3.5" 320x240 Color TFT LCD Module :

◆ Jumper Settings (All jumpers, except JP10 to JP13, can be over-riden by software)

Jumper	Position	Descriptions	Comments
JP10	Open	PLL setting	Default (48MHz)
JP12 – JP11	Close-Close	External SRAM	Select 64kx16 SRAM
JP13	Open	Fonts Flash	Default (no Fonts Flash)
JP17- JP14	Open-Open-Open-Open	Bus interface	Default (8-bit host)
JP20 – JP18	Close-Open-Open	16-bit	Select 5R-6G-5B color depth
JP21	Don't care	-	Select 4/8-bit STN LCD I/F
JP25 – JP22	Close-Open-Open-Open	320x240 LCD	Select LCD size



◆ Pin Mapping

HICDMT04 Board Connector CN1 & CN2		320x240 Color TFT LCD Module Connector A	
Pin	Name	Pin	Name
-	External backlight supply	1,2	VBL- (VSS)
-	External backlight supply	3,4	VBL+ (VBA)
-	-	5,6,	NC
-	External VCOM connection	7	POL
CN1 - 13	LCDPWR (reset control)	8	RST#
CN1 - 6	VDD_3v3	9	SPENA
CN1 - 6	VDD_3v3	10	SPCLK
-	OPEN	11	SPDAT
CN1 - 6	VDD_3v3	12,13,14	B0,B1,B2
CN1 - 9	FD0	15	B3
CN1 - 10	FD1	16	B4
CN1 - 11	FD2	17	B5
CN1 - 12	FD3	18	B6
CN2 - 2	FD4	19	B7
CN1 - 6	VDD_3v3	10,21	G0,G1
CN2 - 3	FD5	22	G2
CN2 - 4	FD6	23	G3
CN2 - 6	FD7	24	G4
CN2 - 7	FD8	25	G5
CN2 - 8	FD9	26	G6
CN2 - 10	FD10	27	G7
CN1 - 6	VDD_3v3	28,29,30	B0,B1,B2
CN2 - 11	FD11	31	B3
CN2 - 12	FD12	32	B4
CN2 - 14	FD13	33	B5
CN2 - 15	FD14	34	B6
CN2 - 16	FD15	35	B7
CN1 - 1	YD	36	HSYNC
CN1 - 2	LP	37	VSYNC
CN1 - 3	XSCL	38	DCLK
CN1 - 15	VDD5	39,40	VDD
CN1 - 6	VDD_3v3	41,42	VCC
-	-	43,44,46,48-50	NC
-	External negative bias voltage	45	VGL
-	External positive bias voltage	47	VGH
-	External VCOM adjustment	51	VCOM
CN1 - 6	VDD_3v3	52	ENB
CN1 - 7	VSS	53,54	GND, AVSS



◆ LCD Module Interface Schematic

